AMENDMENTS TO THE CLAIMS

1. (Currently amended) A metal-oxide-semiconductor (MOS) transistor structure having reduced sheet resistance in the source/drain extensions, comprising:

a gate electrode formed on a semiconductor substrate;

a gate insulating layer formed between the gate electrode and the semiconductor substrate;

a spacer disposed on each sidewall of the gate electrode;

a lightly doped source/drain (S/D) extension formed in the semiconductor substrate under the spacer, the lightly doped S/D extension comprising a raised epitaxial layer bordering bottom of the spacer; wherein the spacer consists of an offset spacer, a liner and a silicon nitride spacer, and wherein the liner directly overlies the epitaxial layer;

a heavily doped S/D region formed in the semiconductor substrate next to an outer edge of the spacer; and

a silicide layer formed on the heavily doped S/D region.

2. (Original) The MOS transistor structure of claim 1 wherein the epitaxial layer has a lattice constant that is greater than the lattice constant of single silicon crystal.

3. (Original) The MOS transistor structure of claim 1 wherein the epitaxial layer serves to increase active concentration and solid solubility of dopants implanted into the lightly doped S/D extension.

4. (Original) The MOS transistor structure of claim3 wherein the dopants are boron.

5. (Original) The MOS transistor structure of claim 1 wherein

the epitaxial layer comprises silicon and germanium.

6. (Original) The MOS transistor structure of claim 5 wherein the epitaxial layer has a germanium molar ratio of 10% to 30%.

7. (Original) The MOS transistor structure of claim 1 wherein the epitaxial layer has a thickness of about 50 to 100 angstroms.

8. (Canceled)

9. (Currently amended) A metal-oxide-semiconductor (MOS) transistor, comprising:

a gate formed on a silicon substrate;

a gate insulating layer formed between the gate and the silicon substrate;

lightly doped source/drain (S/D) extensions formed at both sides of the gate in the silicon substrate, each of the lightly doped S/D extensions comprising a raised epitaxial layer having an active concentration of implanted dopants that is greater than a maximum active concentration of said dopants in the silicon substrate, wherein the epitaxial layer has a germanium molar ratio of 10% to 30%; and

a heavily doped S/D region formed in the silicon substrate and is contiguous with each of the lightly doped S/D extensions.

10. (Original) The MOS transistor of claim 9 wherein the MOS transistor further comprises a spacer disposed on a sidewall of the gate and the raised epitaxial layer is disposed underneath the spacer.

11. (Original) The MOS transistor of claim 9 wherein the

dopants are boron.

12. (Original) The MOS transistor of claim 9 wherein the epitaxial layer has a lattice constant that is greater than the lattice constant of single silicon crystal.

13. (Original) The MOS transistor of claim 9 wherein the epitaxial layer comprises silicon and germanium.

14. (Canceled)

15. (Original) The MOS transistor of claim 9 wherein the epitaxial layer has a thickness of about 50 to 100 angstroms.